IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently amended) A path delay measuring circuitry for judging a signal transition time of a combination circuit whose path delay is to be measured, comprising:

first and a second flip-flop which are connected to an input of the combination circuit and constitute a scan-chain;

a third flip-flop which is connected to an output from said combination circuit to constitute the scan chain;

a pattern creating circuit for creating a test pattern to be set for said first and said second flip-flop;

a comparison/decision circuit for comparing the output from said third flip-flop and the expected value; and

a timing signal creating circuit for supplying an operation timing signal to each of the first, second and third flop-flops, said pattern creating circuit and said comparison/decision circuit,

wherein after a test pattern is set for said first and said second flip-flop by a shifting operation of the scan chain, the output from said combination circuit is taken into said third flip-flop by a capturing operation and an output from said third flip-flop is compared with an expected value~~, and a clock interval of the time taken for the capturing operation is made variable~~, and

wherein said first flip-flop, said second flip-flop and third flip-flop are each clocked utilizing the same clock signal.

2. (Currently amended) A path delay measuring circuitry according to claim 1, further

comprising:

a multiplying circuit for creating a high speed clock on the basis of a clock externally supplied;

a clock mode counter for outputting a clock mode value which is updated whenever said signal transition time is decided; and

a clock creating circuit for creating another clock to be supplied to said path delay measuring circuit on the basis of said high speed clock and said clock mode value,

wherein the clock created by said clock creating circuit is made variable ~~in its clock interval of the time to be taken for said capturing operation according to said clock mode value~~.

3. (Original) A path delay measuring circuitry according to claim 1, wherein a plurality of flip-flops are provided which are identical to said first and second flip-flops.

4. (Original) A path delay measuring circuitry according to claim 2, wherein a plurality of flip-flops are provided which are identical to said first and second flip-flops.

5. (Original) A path delay measuring circuitry according to claim 1, wherein a plurality of flip-flops are provided which are identical to said third flip-flop.

6. (Original) A path delay measuring circuitry according claim 2, wherein a plurality of flip-flops are provided which are identical to said third flip-flop.

7. (Currently amended) A semiconductor device comprising a plurality of path delay measuring circuits, each path delay measuring circuitry judging a signal transition time of a combination circuit whose path delay is to be measured, said path delay measuring circuitry comprising:

first and a second flip-flop which are connected to an input of the combination circuit and constitute a scan-chain;

a third flip-flop which is connected to an output from said combination circuit to constitute the scan chain;

a pattern creating circuit for creating a test pattern to be set for said first and said second flip-flop;

a comparison/decision circuit for comparing the output from said third flip-flop and the expected value; and

a timing signal creating circuit for supplying an operation timing signal to each of the first, second and third flop-flops, said pattern creating circuit and said comparison/decision circuit,

wherein after a test pattern is set for said first and said second flip-flop by a shifting operation of the scan chain, the output from said combination circuit is taken into said third flip-flop by a capturing operation and an output from said third flip-flop is compared with an expected value ~~so that a clock interval of the time taken for the capturing operation is made variable~~, and

wherein said first flip-flop, said second flip-flop and third flip-flop are each clocked utilizing the same clock signal.

8. (Currently amended) A semiconductor device comprising as claimed in claim 7, wherein said path delay measuring circuitry further comprises:

a multiplying circuit for creating a high speed clock on the basis of a clock externally supplied;

a clock mode counter for outputting a clock mode value which is updated whenever said signal transition time is decided; and

a clock creating circuit for creating another clock to be supplied to said path delay

measuring circuit on the basis of said high speed clock and said clock mode value,

wherein the clock created by said clock creating circuit is made variable ~~in its clock interval of the time to be taken for said capturing operation according to said clock mode value~~.